CLAIMS:

1. A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type so formed inside said well as to extend in a first direction x, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and insulated from said first gate through a third insulator film, wherein:

said third gate is so formed as to extend in said first direction x and is buried in a space between said first gates.

2. A semiconductor integrated circuit device according to claim 1, wherein said first gates are formed symmetrically with respect to said third gate, and said third gates are formed symmetrically with respect to said first gate.

3. A semiconductor integrated circuit device according to claim 1, which has any one of the following constructions:

a first construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is an erase gate;

a second construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is a gate for controlling a split channel;

and

a third construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is a gate having the functions of both erase gate and gate for controlling a split channel.

4. A semiconductor integrated circuit device according to claim 3, wherein a part of said third gate exists over said semiconductor region of the second conductivity type.

5. A semiconductor integrated circuit device according to claim 1, wherein said first gate is a floating gate, said second gate is a control gate and said third gate is an erase gate; and

the entire surface of said third gate exists over said semiconductor region of the second conductivity type.

6. A semiconductor integrated circuit device according to claim 1, wherein said third insulator film is a silicon oxide film doped with a nitrogen.

7. A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region so formed inside said well as to extend in a first direction x, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate, wherein:

end faces of said third gate are end faces

opposing said first gates adjacent to each other between said first gates, and are so formed as to oppose end faces of said first gate existing in parallel with said first direction x through said third insulator film.

8. A semiconductor integrated circuit device according to claim 7, which has any of the following constructions:

a first construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is an erase gate;

a second construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is a gate for controlling a split channel; and

a third construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is a gate having the functions of both erase gate and gate for controlling a split channel.

9. A semiconductor integrated circuit device according to claim 8, wherein a part of said third gate exists over said semiconductor region of the second conductivity type.

10. A semiconductor integrated circuit device according to claim 7, wherein said first gate is a floating gate, said second gate is a control gate and said third gate is an erase head, and wherein the entire surface of said third gate exists over said semiconductor region of the second conductivity type.

11. A semiconductor integrated circuit device according to claim 7, wherein said third insulator film is a silicon oxide film doped with nitrogen.

12. A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate over a second insulator film and a third gate formed and isolated from said first gate through a third insulator film , wherein:

an upper surface of said third gate exists at a position lower than the upper surface of said first gate.

13. A semiconductor integrated circuit device according to claim 12, which has any of the following constructions:

a first construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is an erase gate;

a second construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is a gate for controlling a split channel; and

a third construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is a gate having the functions of both erase gate and gate for controlling a split channel.

14. A semiconductor integrated circuit device according to claim 13, wherein a part of said third gate exists over said semiconductor region of the second conductivity type.

15. A semiconductor integrated circuit device according to claim 12, wherein said first gate is a floating gate, said second gate is a control gate and said third gate is an erase gate; and

an entire surface of said third gate exists over said semiconductor region of the second conductivity type.

16. A semiconductor integrated circuit device according to claim 12, wherein said third insulator film is a silicon oxide film doped with nitrogen.

17. A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said third gate has functions of both erase gate and gate for controlling a split channel.

18. A semiconductor integrated circuit device according to claim 17, wherein said third insulator film is a silicon oxide film doped with nitrogen.

19. A semiconductor integrated circuit device

including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and a third gate formed and isolated from said first gate through a third insulator film, wherein:

a film thickness of said first insulator film is greater than that of said second or third insulator film.

20. A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and third gate formed and isolated from said first gate through a third insulator film, wherein:

said second gate comprises a stacked film of a polysilicon film and a metal silicide film, and said third gate exists as it is buried into a space between said first gates.

21. A semiconductor integrated circuit device according to claim 20, wherein said metal silicide film is a tungsten film.

22. A semiconductor integrated circuit device according to claim 20, which has any of the following

constructions:

a first construction wherein the space between said first gates is defined by end faces of said first gates parallel to the extending direction of said second gate among the end faces of said first gates; and

a second construction wherein the space between said first gates is defined by end faces of said first gates vertical to the extending direction of said second gate among the end faces of said first gates.

23. A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said second gate comprises a stacked film containing a metal film.

24. A semiconductor integrated circuit device according to claim 23, wherein said second gate comprises a stacked film of a polysilicon film, a barrier metal film and a metal film.

25. A semiconductor integrated circuit device according to claim 23, wherein said third gate exists as it is buried into the space between said first gates.

26. A semiconductor integrated circuit device

according to claim 23, which as any of the following constructions:

a first construction wherein the space between said first gates is defined by end faces of said first gates parallel to the extending direction of said second gates among the end faces of said first gates; and

a second construction wherein the space between said first gates is defined by end faces of said first gates vertical to the extending direction of said second gates among the end faces of said first gates.

27. A semiconductor integrated circuit device according to claim 24, wherein said barrier metal film belongs to a group of a tungsten film, a titanium film, a tantalum film, a metal film made of a transition metal itself or its nitride film or its silicide film, an aluminum nitride film, a cobalt silicide film, a molybdenum silicide film, a titanium tungsten film or their alloy films.

28. A semiconductor integrated circuit device according to claim 25, which has any of the following constructions:

a first construction wherein the space between said first gates is defined by end faces of said first gates parallel to the extending direction of said second gates among the end faces of said first gates; and

a second construction wherein the space between said first gates is defined by end faces of said first gates vertical to the extending direction of said second

gates among the end faces of said first gates.

29. A semiconductor integrated circuit device including a well of a first conductivity type formed in a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, local source lines and local data lines formed by connecting said semiconductor region, select transistors for selecting said local source line and said local data lines, a first gate formed over said semiconductor integrated substrate through a first insulator film, a second gate formed and isolated from said first gate through a second insulator film, word lines formed by connecting said second gates, and a third gate formed and isolated from said first gate through a third insulator film and having different functions from said first and second gates and, wherein:

a bundling portion of said third gates exists between said word line existing at the nearest position to said select transistor inside a memory cell block comprising said select transistors and the gate of said select transistor.

30. A semiconductor integrated circuit device according to claim 29, wherein a dummy gate exists between said bundling portion of said third gates and said word line existing at the nearest position to said select transistor inside said memory cell block.

31. A semiconductor integrated circuit device according to claim 20, which has any of the following

constructions:

a first construction wherein all of said third gates existing inside said memory cell are bundled at either one, or both of the ends of said memory cell block end; and

a second construction wherein every other of said third gates existing inside said memory cell block are bundled at the memory cell block end.

32. A semiconductor integrated circuit device according to claim 29, wherein all of said third gates existing inside said memory cell block are bundled at either one, or both, of the ends of said memory cell block, and wherein the selection signal of said third gate is generated from a selection signal of said memory cell block.

33. A semiconductor integrated circuit device according to claim 29, wherein all of said third gates existing inside said memory cell block are bundled at either one, or both, of the ends of said memory cell block, said integrated circuit device having any of the following construction:

a first construction wherein the selection signal of said third gate is generated from a selection signal of said memory cell block and a signal for further halving said memory cell block; and

a second construction wherein the selection signal of said third gate is generated from a gate selection signal of said select transistor.

34. A semiconductor integrated circuit device according to claim 30, which has any of the following constructions:

a first construction wherein contact holes are disposed at said bundling portion of said third gates; and

a second construction wherein said third gate and said dummy gate are connected through a contact hole and a metal wire.

35. A semiconductor integrated circuit device according to claim 31, wherein:

said third gate is formed as it is buried into the space between said first gates extending in a direction vertical to said word line; and

a decoder for driving said third gate is disposed in an extending direction of said word line.

36. A semiconductor integrated circuit device according to claim 35, which has any of the following constructions:

a first construction wherein said decoder for driving said third gate is disposed at one of the ends of said memory cell array;

a second construction wherein said decoder for driving said third gate is disposed adjacent to a block decoder for selecting said memory cell block; and

a third construction wherein said decoders for driving said third gate are so disposed on both sides of said memory cell arrays as to interpose said memory cell array between them, adjacent to said block decoder for

selecting said memory cell block.

37. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of a p type;

programming is made by applying a positive voltage relative to voltages of said third gate, said well and a source as one of the regions of said semiconductor region is applied to a control gate as said second gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to a voltage of said control gate to said third gate.

38. An operation method of a semiconductor integrated circuit device according to claim 37, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate during programming.

39. An operation method of a semiconductor

integrated circuit device according to claim 37, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

40. An operation method of a semiconductor device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film:

wherein said well of the first conductivity type is of an n type;

programming is made by applying a negative voltage relative to voltages of said third gate, said well and a source as one of the regions of said semiconductor region to a control gate as said second gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to the voltage of said control gate to said third gate.

41. An operation method of a semiconductor integrated circuit device according to claim 40, wherein the absolute value of the voltage of said third gate is lower than that of the voltage of said control gate.

42. An operation method of a semiconductor

integrated circuit device according to claim 40, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

43. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of an n type;

programming is made by applying a positive voltage relative to voltages of said third gate, said well and a source as one of the regions of said semiconductor region to a control gate as said second gate; and

erasing is made by applying a positive voltage relative to the voltage of said control gate to said third gate.

44. An operation method of a semiconductor integrated circuit device according to claim 43, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate.

45. An operation method of a semiconductor integrated circuit device according to claim 43, wherein a distribution of the threshold value generated by said

programming operation is at least four levels.

46. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of a p type;

programming is made by applying a positive voltage relative to voltages of said third gate and a source as one of the regions of said semiconductor region to a control gate as said second gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a negative voltage relative to the voltage of said well to said control gate while keeping the voltage of said third gate at 0 V.

47. An operation method of a semiconductor integrated circuit device according to claim 46, wherein the absolute value of said third gate is smaller than that of the voltage of said control gate.

48. An operation method of a semiconductor integrated circuit device according to claim 46, wherein a distribution of the threshold voltage generated by said

programming operation is at least four levels.

49. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of a p type;

programming is made by applying a positive voltage relative to voltages of said third gate, said well and a source as one of the regions of said semiconductor region to a control gate as said second gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to the voltage of said control gate to said well.

50. An operation method of a semiconductor integrated circuit device according to claim 49, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate.

51. An operation method of a semiconductor integrated circuit device according to claim 49, wherein a distribution of the threshold voltage generated by said

programming operation is at least four levels.

52. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said gate through a third insulator film, wherein:

said well of the first conductivity type is of an n type;

programming is made by applying a negative voltage relative to voltages of said well and a source as one of the regions of said semiconductor region to a control gate as said second gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a negative voltage relative to the voltage of said well to said control gate while the voltage of said third gate is kept at 0 V.

53. An operation method of a semiconductor integrated circuit device according to claim 52, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate.

54. An operation method of a semiconductor integrated circuit device according to claim 52, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

55. An operation method of a semiconductor

integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of an n type;

programming is made by applying a negative voltage relative to voltages of said third gate, said well and a source as one of the regions of said semiconductor layer to a control gate as said second gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to the voltage of said control gate to said well.

56. An operation method of a semiconductor integrated circuit device according to claim 55, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate.

57. An operation method of a semiconductor integrated circuit device according to claim 55, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

58. An operation method of a semiconductor integrated circuit device including a well of a first

conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of a p type;

programming is made by applying a positive voltage relative to voltages of said well and a source as one of the regions of said semiconductor region to a control gate as said second gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to the voltage of said control gate to said third gate.

59. An operation method of a semiconductor integrated circuit device according to claim 58, wherein the absolute value of said third gate is smaller than that of the voltage of said control gate during said programming operation.

60. An operation method of a semiconductor integrated circuit device according to claim 58, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

61. An operation method of a semiconductor

integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of a p type;

programming is made by applying a positive voltage relative to voltages of said well and a source as one of the regions of said semiconductor region to a control gate as said second gate, to said third gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a negative voltage relative to the voltage of said well to said control gate.

62. An operation method of a semiconductor integrated circuit device according to claim 61, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate during said programming operation.

63. An operation method of a semiconductor integrated circuit device according to claim 61, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

64. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of a p type;

programming is made by applying a positive voltage relative to voltages of said well and a source as one of the regions of said semiconductor region to a control gate as said second gate, to said third gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to the voltage of said control gate to said well.

65. An operation method of a semiconductor integrated circuit device according to claim 64, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate during said programming operation.

66. An operation method of a semiconductor integrated circuit device according to claim 64, wherein a distribution of the threshold voltage generated by said

programming operation is at least four levels.

67. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of a p type;

programming is made by applying a positive voltage relative to voltages of said well and a source as one of the regions of said semiconductor region to a control gate as said second gate, to said third gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to a voltage of said control gate to said source or said drain.

68. An operation method of a semiconductor integrated circuit device according to claim 67, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate during said programming operation.

69. An operation method of a semiconductor

integrated circuit device according to claim 67, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

70. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of an n type;

programming is made by applying a negative voltage relative to voltages of said well and a source as one of the regions of said semiconductor region to a control gate as said second gate, to said third gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to the voltage of said control gate to said third gate.

71. An operation method of a semiconductor integrated circuit device according to claim 70, wherein the absolute value of the voltage of said third gate is smaller than that of the voltage of said control gate

during said programming operation.

72. An operation method of a semiconductor integrated circuit device according to claim 70, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

73. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of an n type;

programming is made by applying a negative voltage relative to voltages of said well and a source as one of the regions of said semiconductor region to a control gate as said second gate, to said third gate and to a drain as the other region of said semiconductor region; and

erasing is made by applying a negative voltage relative to the voltage of said well to said control gate.

74. An operation method of a semiconductor integrated circuit device according to claim 73, wherein the absolute value of the voltage of said third gate is

smaller than that of the voltage of said control gate during said programming operation.

75. An operation method of a semiconductor integrated circuit device according to claim 73, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

76. An operation method of a semiconductor integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulation film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said well of the first conductivity type is of an n type;

programming is made by applying a negative voltage relative to said well and a source as one of the regions of said semiconductor region to a control gate as said second gate and a drain as the other region of said semiconductor region; and

erasing is made by applying a positive voltage relative to the voltage of said control gate to said well.

77. An operation method of a semiconductor integrated circuit device according to claim 76, wherein an absolute value of said third gate is smaller than that

of the voltage of said control gate during said programming operation.

78. An operation method of a semiconductor integrated circuit device according to claim 76, wherein a distribution of the threshold value generated by said programming operation is at least four levels.

79. A method of producing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a well of a first conductivity type in a semiconductor substrate;

(b) forming a stripe-like pattern to serve as a first gate over said semiconductor substrate through a first insulator film;

(c) forming a semiconductor region of a second conductivity type inside said well in such a manner as to extend in parallel with said pattern;

(d) forming a third insulator film in the space defined by said stripe-like pattern, and burying a third gate into said space of said pattern; and

(e) forming a second gate pattern in such a manner as to extend in a direction vertical to said stripe-like pattern.

80. A method of producing a semiconductor integrated circuit device according to claim 79, wherein said strip-like pattern to function as said first gate is patterned in such a manner as to be symmetric with respect to said third gate, and said third gate is patterned in such a manner as to be symmetric with respect to said stripe-like

pattern.

81. A method of producing a semiconductor integrated circuit device according to claim 79, which has any of the following methods:

a first method of forming said third gate in such a manner that the entire surface of said third gate exists over said semiconductor region of the second conductivity type; and

a second method of forming said third gate in such a manner that a part of said third gate exists over said semiconductor region of the second conductivity type.

82. A method of producing a semiconductor integrated circuit device according to claim 79, wherein said third gate is formed in such a manner that a part thereof exists over said semiconductor region of the second conductivity type, and said semiconductor region of the second conductivity type is formed by tilted ion implantation.

83. A method of producing a semiconductor integrated circuit device according to claim 79, wherein said third insulator film is a silicon oxide film doped with nitrogen.

84. A method of producing a semiconductor integrated circuit device according to claim 80, wherein said third gate is formed in self-alignment with said stripe-like pattern.

85. A method of producing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a well of a first conductivity type inside a semiconductor substrate;

(b) forming a first gate over said semiconductor substrate through a first insulator film;

(c) forming a semiconductor region of a second conductivity type inside said well;

(d) forming a third insulator film in a space defined by said first gate, and forming said third gate in such a manner as to bury the space of said pattern; and

(e) forming a second gate;

wherein said third gate is patterned so that the surface of said third gate is lower than the surface of said first gate.

86. A method of producing a semiconductor integrated circuit device according to claim 85, which has any of the following methods:

a first method of forming said third gate so that the entire surface of said third gate exists over said semiconductor region of the second conductivity type; and

a second method of forming said third gate so that a part of said third gate exists over said semiconductor region of the second conductivity type.

87. A method of producing a semiconductor integrated circuit device according to claim 85, wherein said third gate is formed in such a manner that a part of said third gate exists over said semiconductor region of the second conductivity type, and said semiconductor region of the second conductivity type is formed by tilted ion implantation.

88. A method of producing a semiconductor integrated circuit device according to claim 85, wherein said third insulator film is a silicon oxide film doped with nitrogen.

89. A method of producing a semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said second gate comprises a laminate film of a polysilicon film and a metal silicide film, and the formation of said second gate is conducted after the formation of said third gate.

90. A method of producing a semiconductor integrated circuit device according to claim 89, wherein said metal silicide film is a tungsten silicide film.

91. A semiconductor integrated circuit device including a well of a first conductivity type formed in a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, local source lines and local data lines formed by connecting said semiconductor region , select transistors for selecting said local source lines and said local data lines, a first gate formed over said semiconductor substrate through a first insulator film, a second gate

formed and isolated from said first gate through a second insulator film, word lines formed by connecting said second gates, and memory cells existing on said local source lines and said local data lines divided by said select transistors forming a memory cell block, said memory cell blocks being arranged in the direction of said word lines and constituting a memory cell array, wherein:

one each power source line is disposed on both sides of said memory cell block to interpose said memory cell block in the same direction as said word lines; and

said local source line and said local data line are connected to one of said power source lines and to a signal line arranged in a direction vertical to said word line, or to both of said power source lines, through said select transistor.

92. A semiconductor integrated circuit device according to claim 91, which has any of the following constructions:

a first construction wherein one of said local data lines is connected to both of said power source line and said signal line through said select transistor; and

a second construction wherein one of said local data lines is connected to said signal line at one of the ends of said memory cell block through said select transistor, and an adjacent local data line adjacent to said one local data line is connected to said signal line at the other end of said memory cell block through said select transistor.

93. A semiconductor integrated circuit device according to claim 91, which has any of the following constructions:

a first construction wherein a gate signal of said select transistor connected to said local source line and a gate signal of said select transistor connected to said local data line are the same signal; and

a second construction wherein gate signals of all of said select transistors connected to said local source lines are the same signal.

94. A semiconductor integrated circuit device according to claim 92, wherein one of said local data lines is connected to said signal line at one of the ends of said memory cell block through said select transistor and to said power source line at the other end of said memory cell block through said select transistor.

95. A semiconductor integrated circuit device according to claim 94, which includes a first select transistor for connecting a signal line disposed in a direction vertical to the extending direction of said word line to an nth (n: integer) local data line, a second select transistor for connecting said power source line disposed at one of the ends of said memory cell block in the same direction as said word line to (n+1)th local data line, a third select transistor for connecting said signal line to said (n+1)th local data line, and a fourth select transistor for connecting said power source line disposed at the other end of said memory cell block in the same

direction as said word line to said nth local data line, wherein:

the gate signals of said first and second transistors are the same signals; and

the gate signal of said third and fourth select transistors are the same signal.

96. A semiconductor integrated circuit device including a well of a first conductivity type formed in a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, local source/data lines formed by connecting said semiconductor region, select transistors for selecting said local source/data lines, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed and isolated from said first gate through a second insulator film, and word lines formed by connecting said second gate, wherein:

memory cells on said local source/data lines divided by said select transistors constitute memory cell blocks, and said memory cell blocks are arranged in said word line direction and constitute a memory cell array; and

when said local source/data lines function as the local source lines of said memory cell, they function as the local data line of said memory cells adjacent to said memory cell;

said semiconductor integrated circuit device including further:

one each power source line so disposed on both sides of said memory cell block as to interpose said memory cell block between them in the same direction as said word line, and signal lines disposed in a direction vertical to said word lines;

said local source/data lines being connected to either one of said power source lines and to both of said signal lines through said select transistor.

97. A semiconductor integrated circuit device according to claim 96, which has any of the following constructions:

a first construction wherein nth (n: integer) local source/data line is connected to said signal line at one of the ends of said memory cell block through said select transistor and (n+1)th local source/data line is connected to said signal line at the other end of said memory cell block through said select transistor; and

a second construction wherein an nth (n: integer) local source/data line is connected to said power source line at one of the ends of said memory cell block through said select transistor, and an (n+1)th local source/data line is connected to said power source line at the other end of said memory cell block through said select transistor.

98. A semiconductor integrated circuit device according to claim 96, wherein one of said local source/data lines is connected to said signal line at one of the ends of said memory cell block through said select

transistor, and to said power source line at the other end of said memory cell block through said select transistor.

99. A semiconductor integrated circuit device according to claim 96, which has any of the following constructions:

a first construction wherein one of said signal lines wired in a direction vertical to said word line is shared by two of said local source/data lines;

a second construction wherein, when said local source/data line is connected to said signal line through said select transistor, the connection portion between the semiconductor region of said select transistor on the side different from said local source/data line and said signal line is shared by two of said memory cell blocks; and

a third construction wherein said power source line is shared by two of said memory cell blocks.

100. A semiconductor integrated circuit device according to claim 98, which further includes a first select transistor for connecting said signal line wired in a direction vertical to said word line and an nth (n: integer) local source/data line, a second select transistor for connecting said power source line wired at one of the ends of said memory cell block in the same direction as said word line and an (n+1)th local source/data line, a third select transistor for connecting said signal line and said (n+1)th local source/data line and a fourth select transistor for connecting said power source line wired at the other end of said memory cell

block in the same direction as said word line and said nth local source/data line, wherein:

the gate signals of said first and second select transistors are the same signal, and the gate signals of said third and fourth select transistors are the same signal.

101. A semiconductor integrated circuit device including a well of a first conductivity type formed in a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, local source/data lines formed by connecting said semiconductor regions, select transistors for selecting said local source/data lines, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed and isolated from said first gate through a second insulator film, word lines formed by connecting said second gates, and a third gate formed and isolated from said first gate through a third insulator film and having a different function from those of said first and second gates, memory cells on said local source lines and local data lines divided by said select transistors constituting memory cell blocks, said memory cell blocks being arranged in the word line direction and constituting a memory cell array, wherein:

a bundling portion of said third gates exists between said word line existing at the nearest position to said select transistor inside said memory cell block and the gate of said select transistor;

every other third gates existing inside said memory cell block are bundled at one of the ends of said memory cell block;

one each power source line are so disposed in the same direction as said word lines on both sides of said memory cell block as to interpose said memory cell block between them, and signal lines disposed in a direction vertical to said word lines; and

said local source/data lines are connected to either one, or both, of said signal lines inside said power source line through said select transistor.

102. A semiconductor integrated circuit device according to claim 101, which has any of the following constructions:

a first construction wherein an nth (n: integer) local source/data line is connected to said signal line at one of the ends of said memory cell block through said select transistor, and an (n+1)th local source/data line is connected to said signal line at the other end of said memory cell block through said select transistor; and

a second construction wherein an nth (n: integer) local source line is connected to said power source line at one of the ends of said memory cell block through said select transistor, and an (n+1)th local source/data line is connected to said power source line at the other end of said memory cell block through said select transistor.

103. A semiconductor integrated circuit device

according to claim 101, wherein one of said local source/data lines is connected to said signal line at one of the ends of said memory cell block through said select transistor, and is connected to said power source line at the other end of said memory cell block through said select transistor.

104. A semiconductor integrated circuit device according to claim 101, which has any of the following constructions:

a first construction wherein one of said signal lines disposed in a direction vertical to said word line is shared by two of said local source/data lines;

a second construction wherein, when said local source/data line and said signal line are connected through said select transistor, the connection portion between said semiconductor region of said select transistor on the side different from said local source/data line and said signal line is shared by two of said memory cell blocks;

a third construction wherein said power source line is shared by two of said memory cell blocks;

a fourth construction wherein said local source/data line is connected to said signal line wired in a direction vertical to said word line through said select transistor, a sense circuit is connected to said signal line, said sense circuit connected to an nth (n: integer) signal line is connected at one of the ends of a memory cell array comprising a plurality of memory cell blocks,

and said sense circuit connected to an (n+1)th signal line is connected at the other end of said memory cell array; and

a fifth construction wherein a switch is interposed between said signal line connected to said local source/data line through said select transistor and said sense circuit, and one sense circuit can be shared by a plurality of said signal lines when said switch is changed over.

105. A semiconductor integrated circuit device according to claim 103, which further includes a first select transistor for connecting a signal line wired in a direction vertical to said word line and an nth (n: integer) local source/drain line, a second select transistor for connecting said power source line wired in the same direction as said word line to one of the ends of said memory cell block and an (n+1)th local source/data line, a third select transistor for connecting said signal line and said (n+1)th local source/date line and a fourth select transistor for connecting said power source line wired in the same direction as said word line and said nth local source/data line to the other end of said memory cell block, wherein:

the gate signals of said first and second select transistors are the same signal; and

the gate signals of said third and fourth select transistors are the same signal.

106. A semiconductor integrated circuit device

including a well of a first conductivity type formed in a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, local source/data lines formed by connecting said semiconductor region, select transistors for selecting said local source/data lines, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed and isolated from said gate through a second insulator film, word lines formed by connecting said second gates, and a third gate formed and isolated from said first gate through a third insulator film and having a different function from those of said first and second gates, memory cells on said local source lines and said local data lines divided by said select transistors constituting a memory cell block, said memory cell blocks being arranged in the word line direction and constituting a memory cell array, wherein:

a bundling portion of said third gates exists between said word line existing at the nearest position to said select transistor inside said memory cell block and said select transistor;

every other third gates existing inside said memory cell block are bundled at the end of said memory cell block;

one each of said power source line arranged in the same direction as said word line and one each of said signal lines wired in a direction vertical to said word lines are so disposed on both sides of said memory cell

block as to interpose said memory cell block between them; and

said local source/data line is connected to both of said power source line and said signal line through said select transistor.

107. A semiconductor integrated circuit device according to claim 106, which has any of the following constructions:

a first construction wherein said local source/data line is connected to said signal line through said select transistor, and said connection is all made at one of the ends of said memory cell block; and

a second construction wherein said local source/data line is connected to said power source line wired in the same direction as said word line at one of the ends of said cell block through said select transistor, and said connection is all made at one of the ends of said memory cell block.

108. A semiconductor integrated circuit device according to claim 106, wherein one of said local source/data line is connected to said signal line at one of the ends of said memory cell block through said select transistor, and is connected to said power source line at the other end of said memory cell block through said select transistor.

109. A semiconductor integrated circuit device according to claim 106, which has any of the following constructions:

a first construction wherein two of said local source/data lines share said signal line;

a second construction wherein, when said local source/data line and said signal line are connected through said select transistor, the connection portion of the semiconductor region of said select transistor on the side different from said local source/data line and said signal line is shared by two of said memory cell blocks;

a third construction wherein two of said memory cell blocks share said power source line;

a fourth construction wherein said local source/data line is connected to said signal line through said select transistor, said sense circuit is connected to said signal line, said sense circuit to be connected to nth (n: integer) signal line is connected at one of the ends of said memory cell array comprising a plurality of memory cell blocks, said sense circuit to be connected to (n+1)th signal line is connected at the other end of said memory cell array; and

a fifth construction wherein a switch is interposed between said signal line connected to said local source/data line through said select transistor and said sense circuit, and one sense circuit is shared by a plurality of said signal lines as said switch is changed over.

110. A semiconductor integrated circuit device according to claim 108, which further includes a first select transistor for connecting said signal line wired in

a direction vertical to said word line and an nth (n: integer) local source/data line, a second select transistor for connecting said signal line and an (n+1)th local source/data line, a third select transistor for connecting said power source line wired in the same direction as said word line and said nth local source/data line at the other end of said memory cell block, and a fourth select transistor for connecting said power source line and said (n+1)th local source/data line, wherein:

the gate signals of all of said first select transistors are the same signal;

the gate signals of all of said second select transistors are the same signal;

the gate signals of said first and second select transistors are different signals, and the gate signals of all of said third select transistors are the same signal;

the gate signals of all of said fourth select transistors are the same signal; and

the gate signals of said third and fourth gate signals are different signals.

111. A semiconductor integrated circuit device including a well of a first conductivity type formed in a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well in such a manner as to extend in a first direction, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film, word

lines formed by connecting said second gate, and a third gate formed and isolated from said first gate through a third insulator film, said third gate being buried in a space of said first gate existing in a direction vertical to said word line, wherein:

a decoder for driving said third gate is disposed in the extending direction of said word line.

112. A semiconductor integrated circuit device according to claim 111, which has any of the following constructions:

a first construction wherein said decoder for driving said third gate is disposed at one of the ends of a memory cell array;

a second construction wherein said decoder for driving said third gate is disposed adjacent to a block decoder for selecting memory cell blocks each comprising memory cell arrays existing on a plurality of word lines encompassed by said select transistors; and

a third construction wherein said decoders for driving said third gates are disposed on both sides of said memory cell while interposing said memory cell array between them and adjacent to a block decoder for selecting said memory cell blocks.